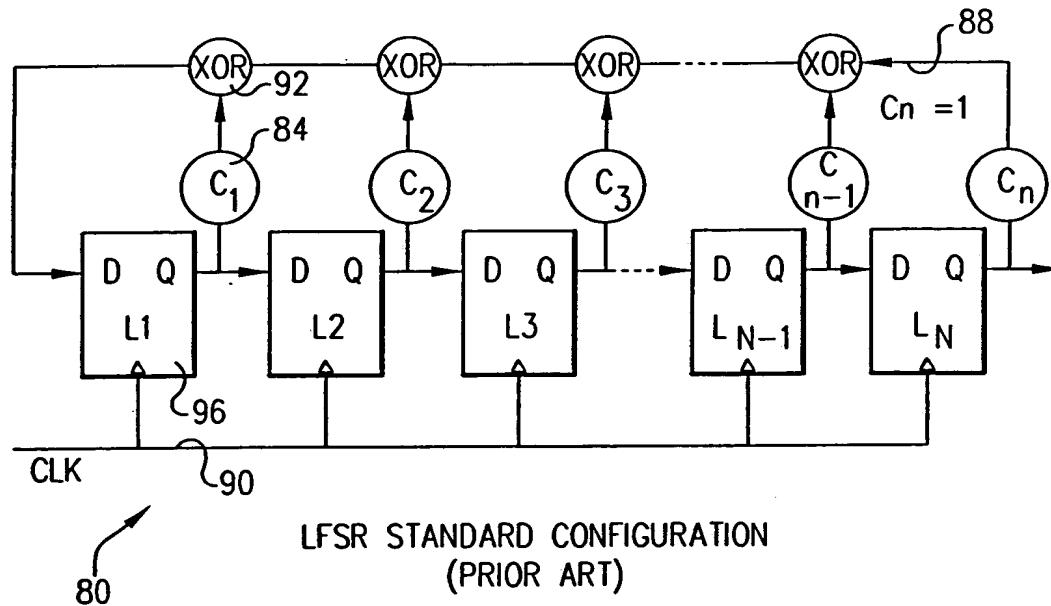


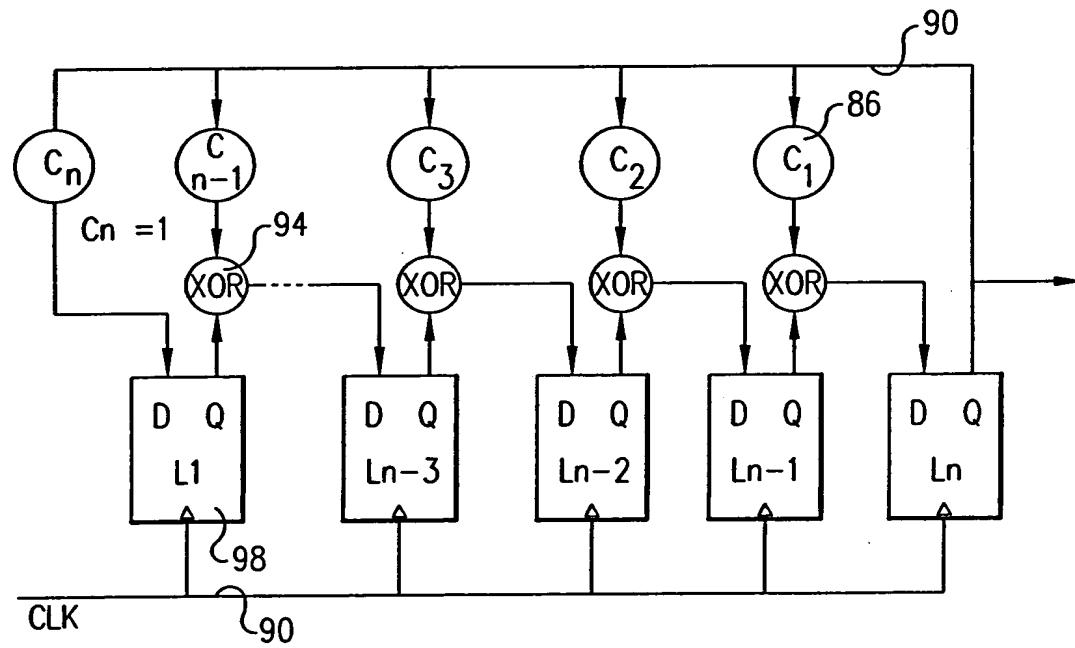
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LFSR STANDARD CONFIGURATION  
 (PRIOR ART)

FIG. 1

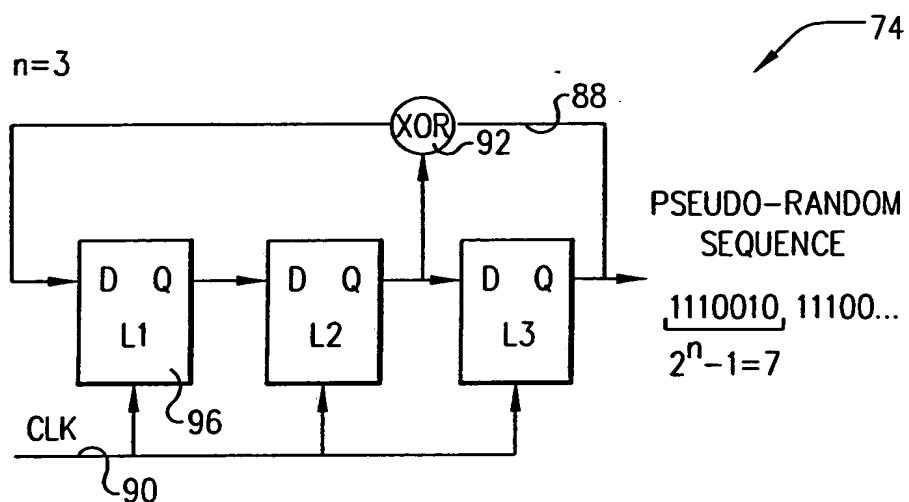


LFSR MODULAR CONFIGURATION  
 (PRIOR ART)

FIG. 2

MODULO-2 ADD & SUB. TRUTH TABLE	
+/-	0 1
0	0 1
1	1 0

FIG. 3  
PRIOR ART



$S_0$	1		1		1
$S_1$	0		1		1
$S_2$	0		0		1
$S_3$	1		0		0
$S_4$	0		1		0
$S_5$	1		0		1
$S_6$	1		1		0
$S_0$	1		1		1

STATE TABLE

78

FIG. 4  
PRIOR ART

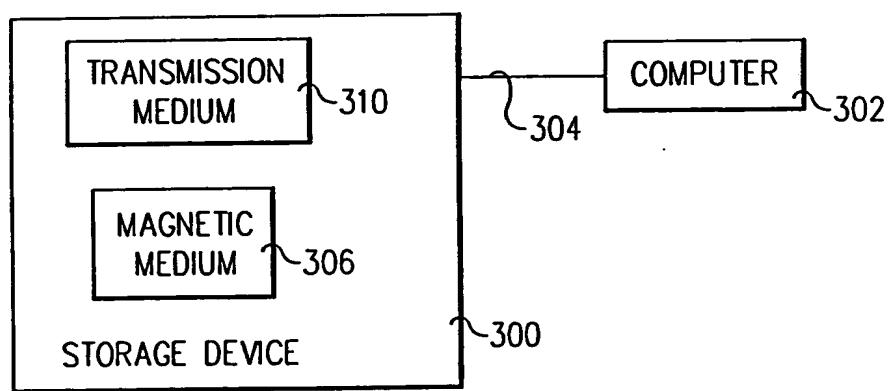
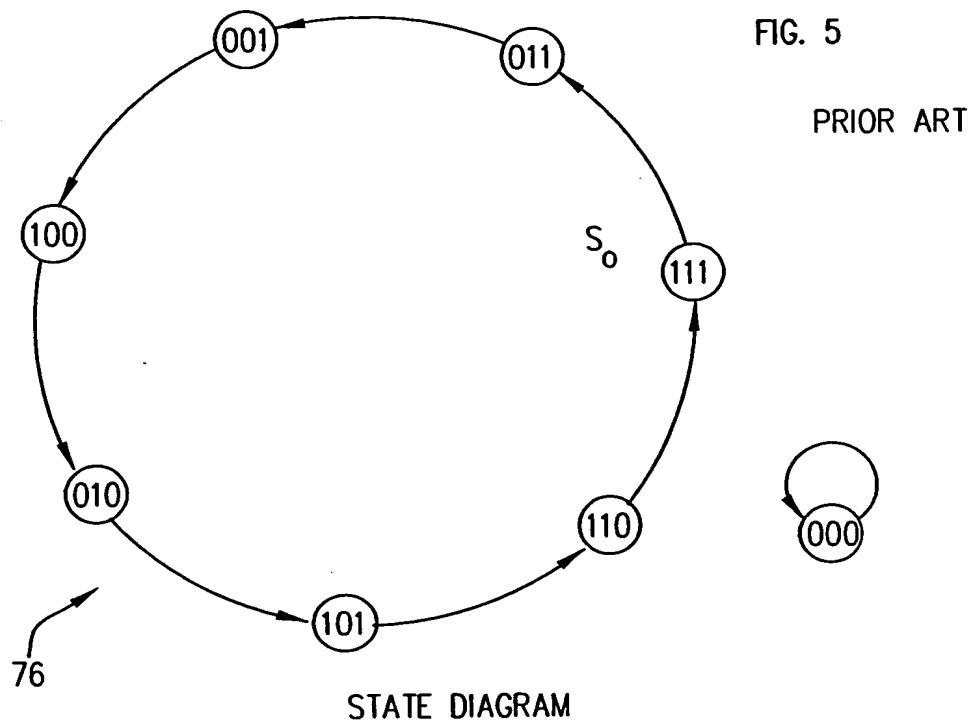
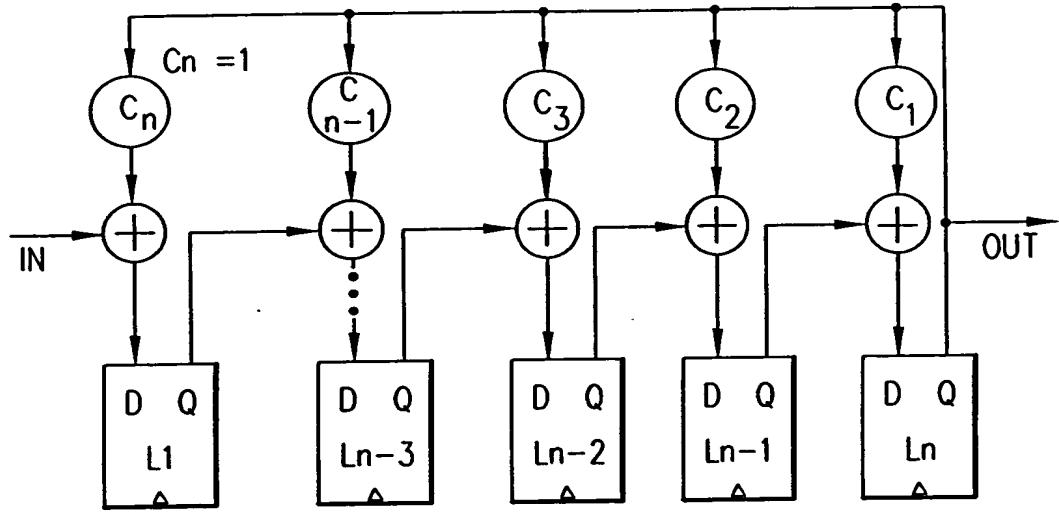
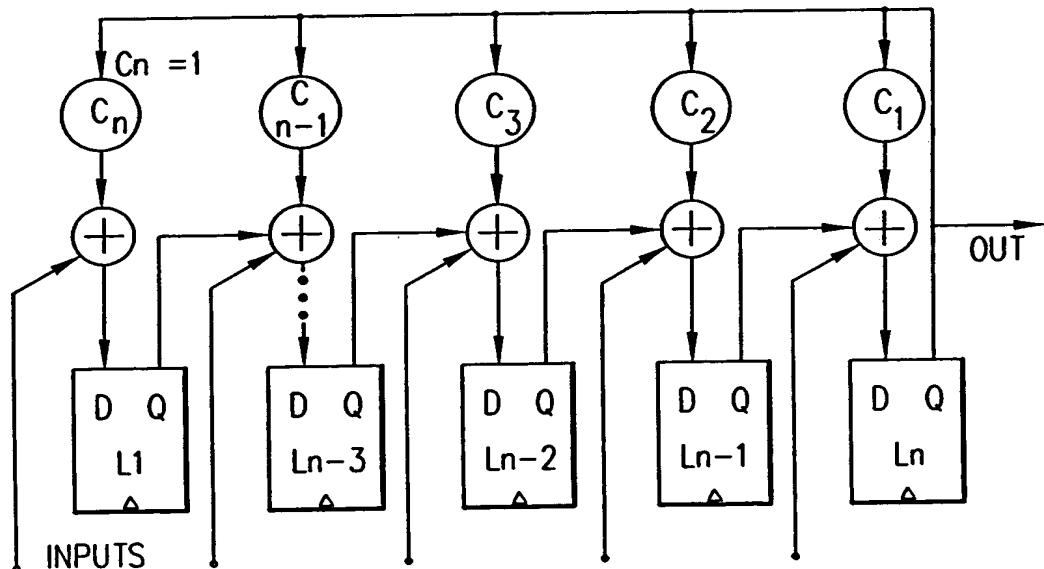


FIG. 17



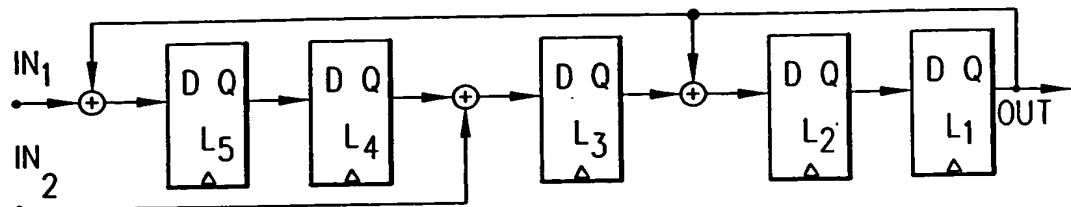
SINGLE INPUT SIGNATURE REGISTER (SISR)

FIG. 6  
PRIOR ART



MULTIPLE INPUT SIGNATURE REGISTER (MISR)

FIG. 7  
PRIOR ART



MAXIMAL LENGTH LFSR  
MULTIPLE INPUT SIGNATURE REGISTER (MISR)

FIG. 8  
PRIOR ART

	L <sub>5</sub>	L <sub>4</sub>	L <sub>3</sub>	L <sub>2</sub>	L <sub>1</sub>
0	1	1	1	1	1
1	1	1	1	0	1
2	1	1	1	0	0
3	0	1	1	1	0
4	0	0	1	1	1
5	1	0	0	0	1
6	1	1	0	1	0
7	0	1	1	0	1
8	1	0	1	0	0
9	0	1	0	1	0
10	0	0	1	0	1
11	1	0	0	0	0
12	0	1	0	0	0
13	0	0	1	0	0
14	0	0	0	1	0
15	0	0	0	0	1
16	1	0	0	1	0
17	0	1	0	0	1
18	1	0	1	1	0
19	0	1	0	1	1
20	1	0	1	1	1
21	1	1	0	0	1
22	1	1	1	1	0
23	0	1	1	1	1
24	1	0	1	0	1
25	1	1	0	0	0
26	0	1	1	0	0
27	0	0	1	1	0
28	0	0	0	1	1
29	1	0	0	1	1
30	1	1	0	1	1
	1	1	1	1	1

FIG. 9  
PRIOR ART

	IN1	IN2	L <sub>5</sub>	L <sub>4</sub>	L <sub>3</sub>	L <sub>2</sub>	L <sub>1</sub>
0	0	1	1	1	1	1	1
1	1	1	1	1	1	0	1
2	0	1	1	0	0	0	1
3	1	1	0	0	1	0	1
4	0	0	1	0	0	1	1
5	0	0	1	1	0	0	0
6	1	1	1	1	0	0	0
7	1	1	1	1	0	0	0
8	0	0	0	1	1	0	0
9	0	1	0	0	0	1	0
10	1	0	1	0	0	0	1
11	1	0	0	1	0	0	1
12	0	0	1	0	1	0	1
13	0	0	1	1	0	1	1
14	0	0	1	1	1	0	0
15	1	0	1	1	1	1	0
16	1	0	1	1	1	1	1
17	1	1	0	1	0	1	0
18	0	1	0	0	0	0	1
19	0	1	1	0	1	0	1
20	0	1	1	1	1	1	1
21	0	1	1	1	0	1	0
22	1	1	1	1	1	0	1
23	1	1	0	1	0	1	1
24	1	0	0	0	0	0	0
25	1	1	1	0	1	0	0
26	0	1	0	1	0	1	0
27	0	0	0	0	0	0	1
28	0	1	1	0	1	0	1
29	0	0	1	1	1	1	1
30	0	1	1	1	0	1	0

FIG. 10  
PRIOR ART

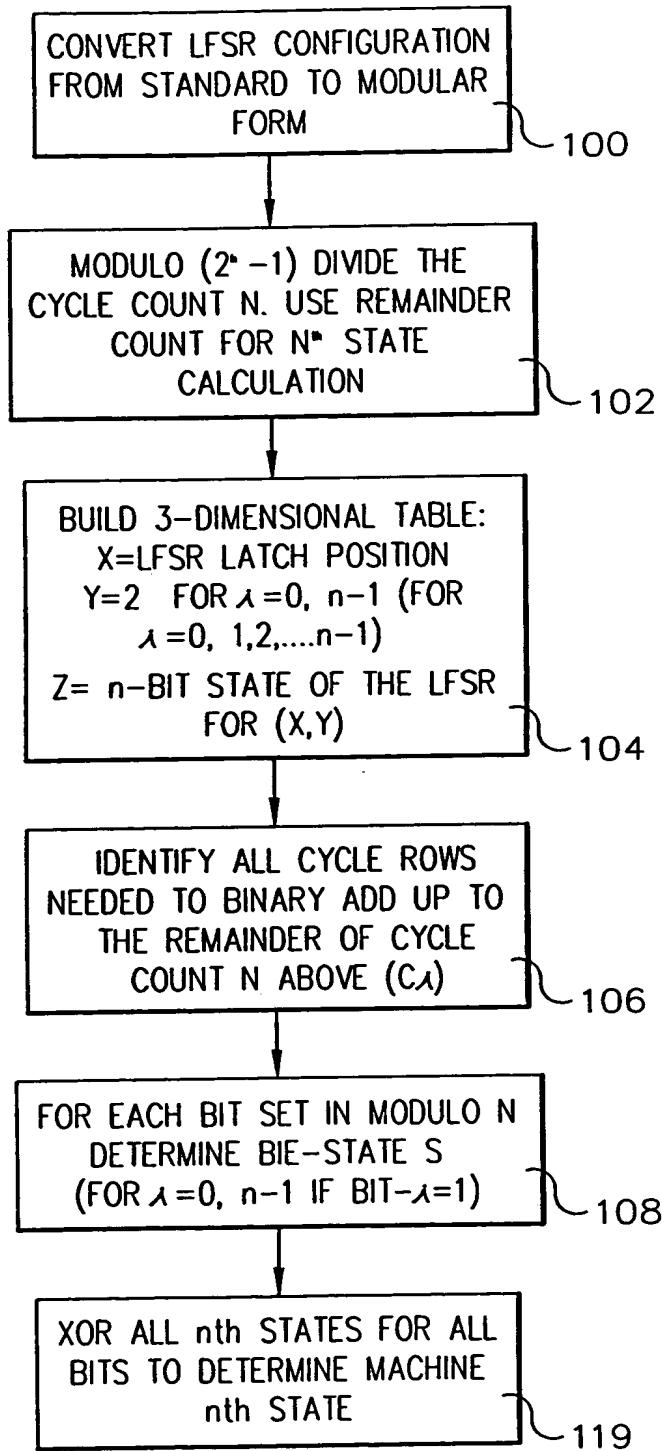


FIG. 11

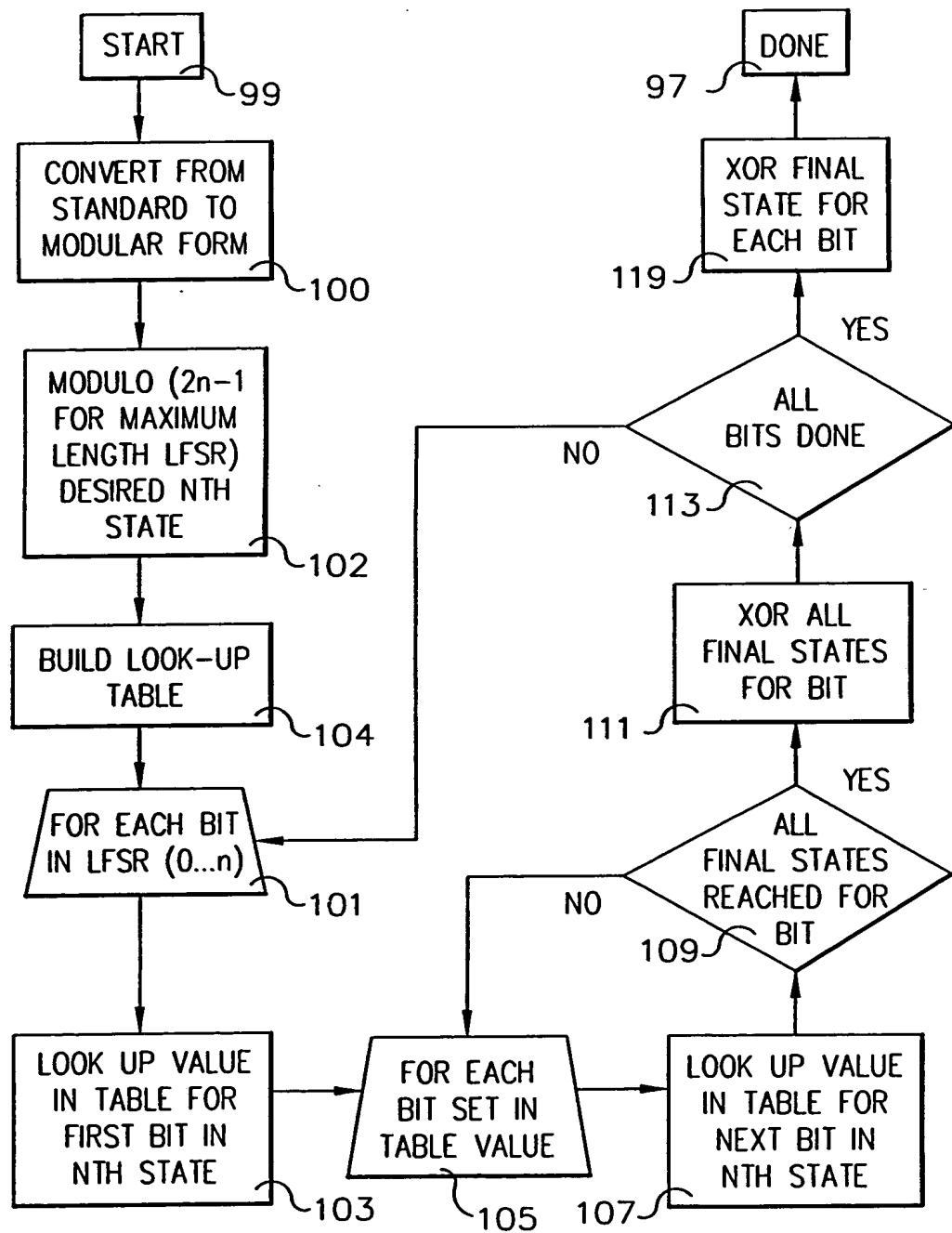
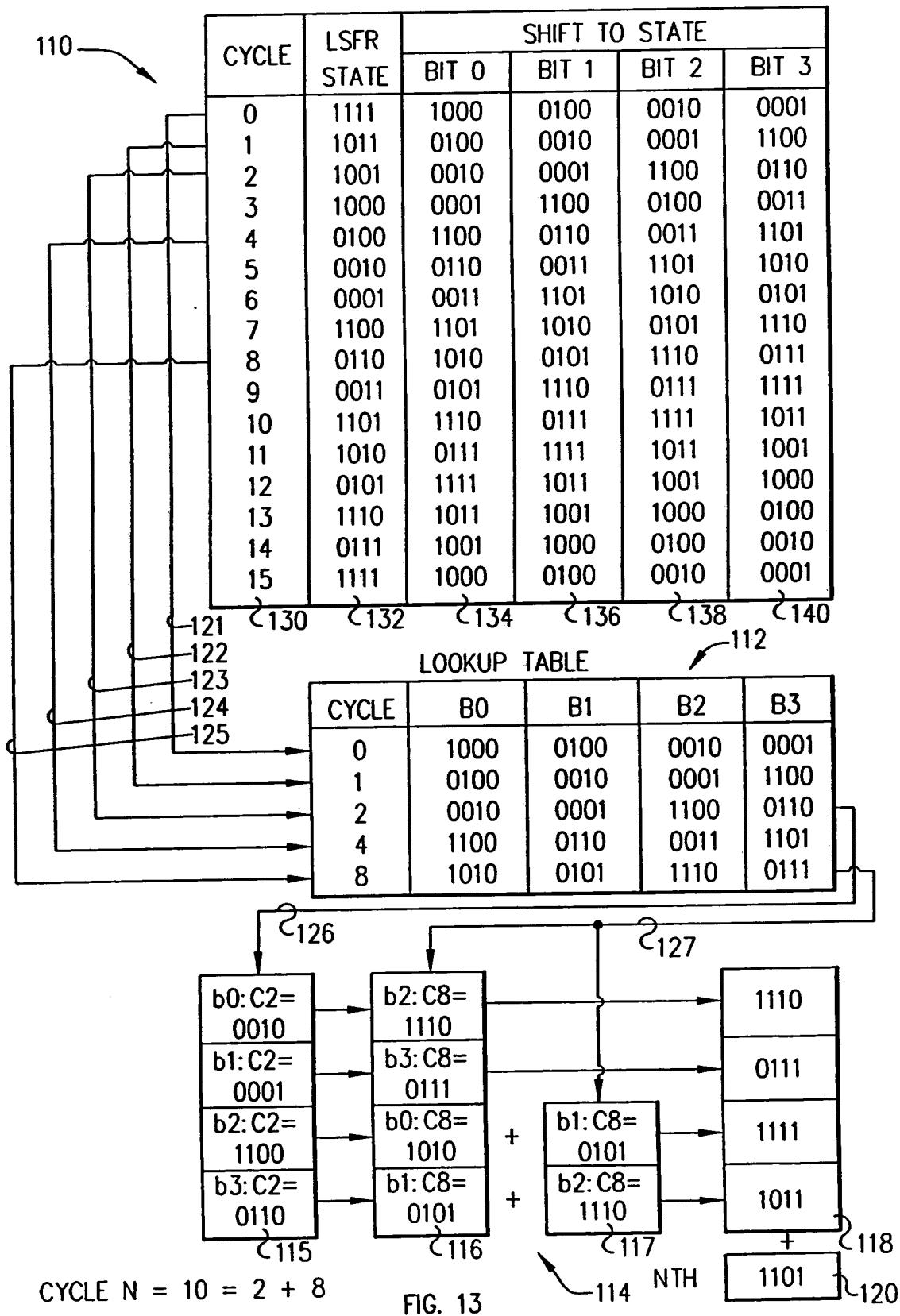


FIG. 12



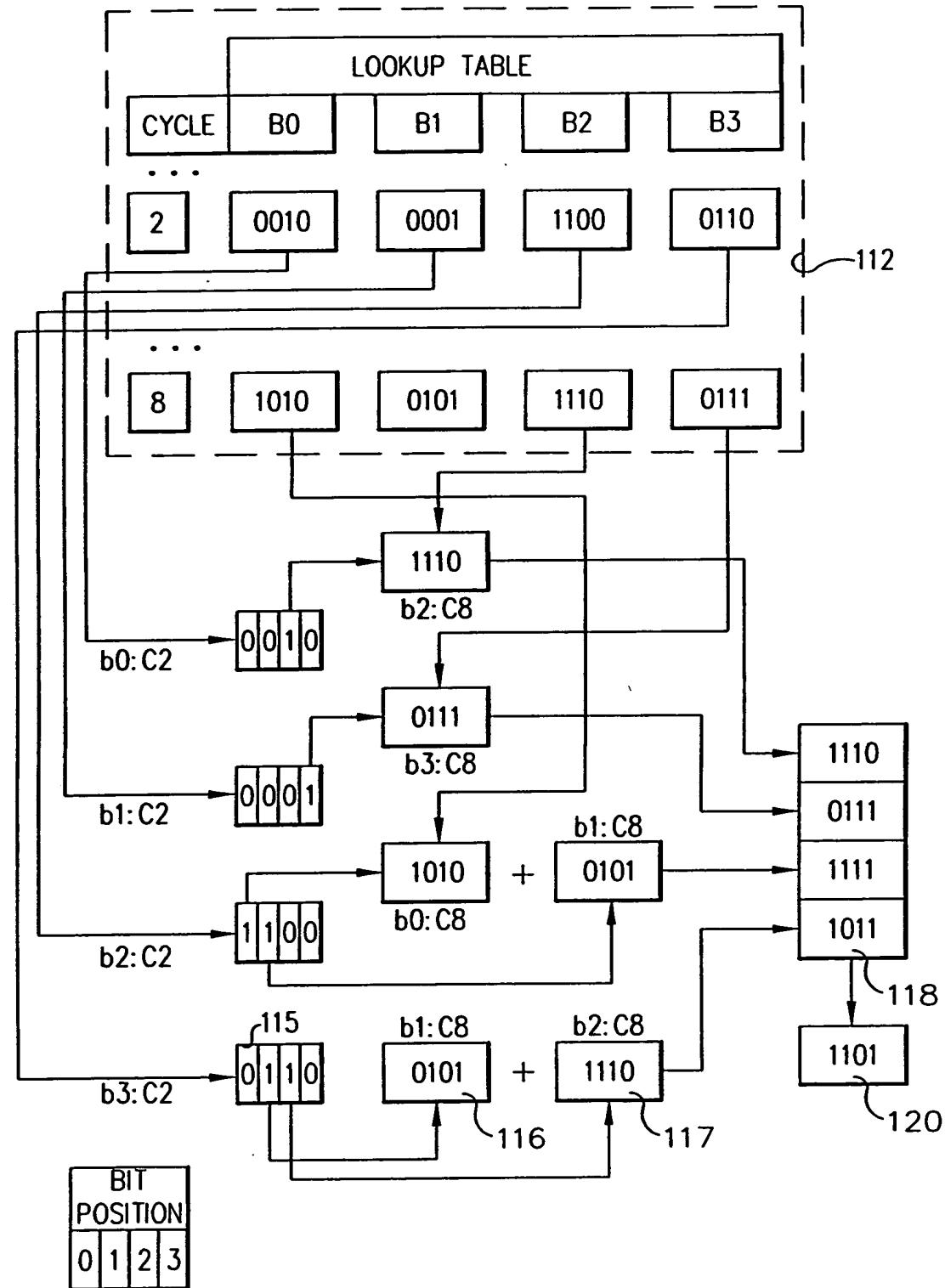


FIG. 14

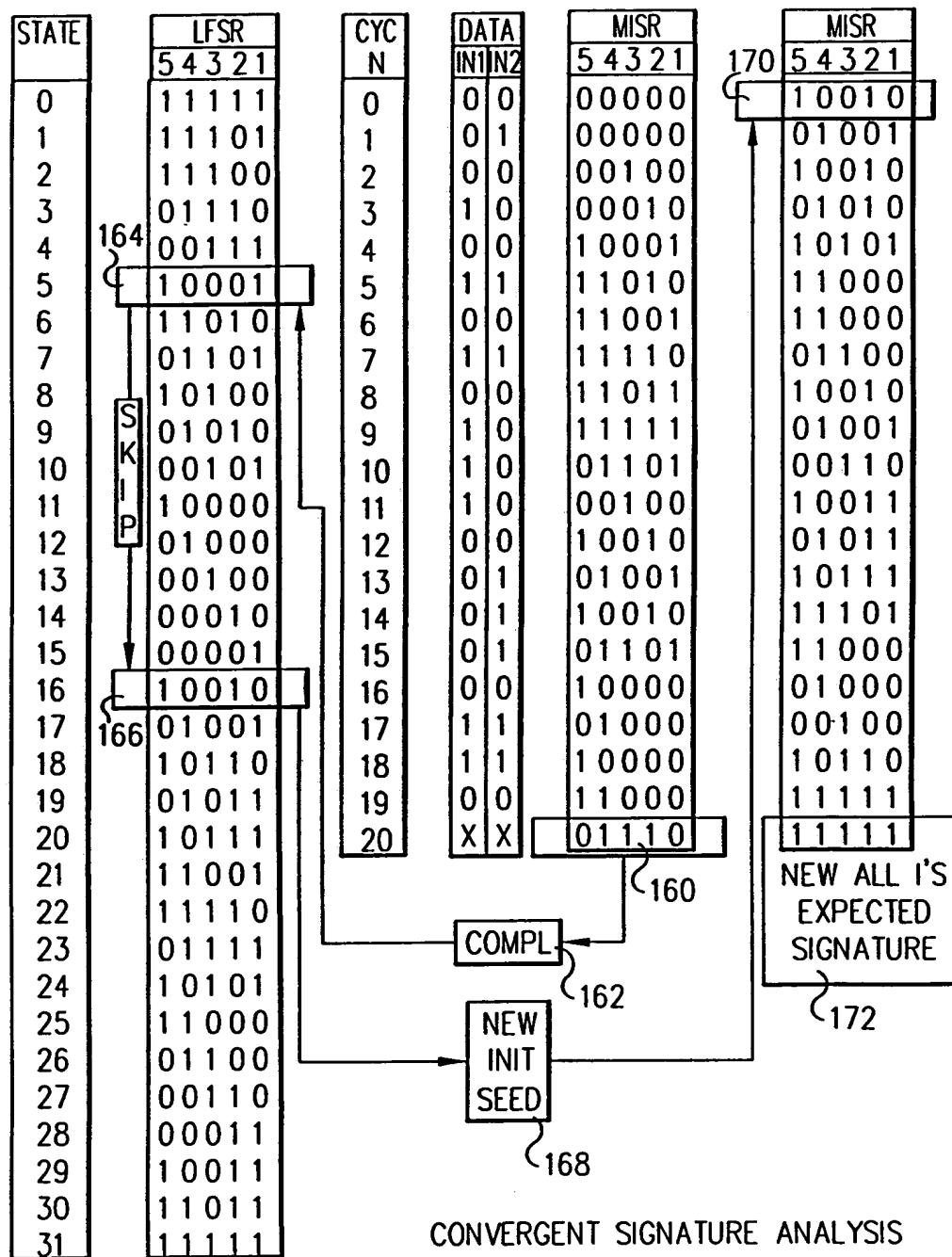


FIG. 15

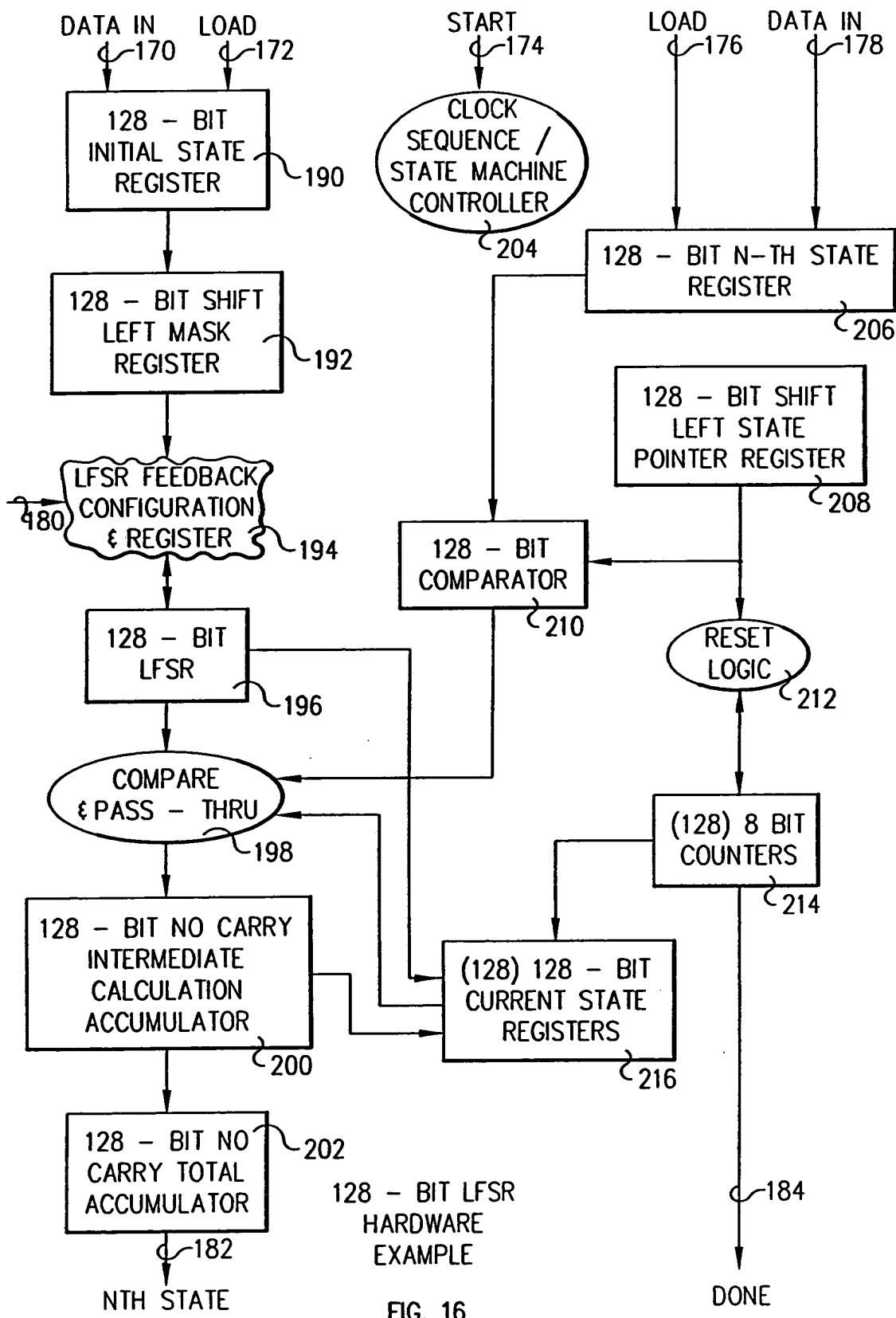


FIG. 16